DR068

## Digitising Receiver

The DR068 latest Digitising Receiver builds on the strong tradition of TDL Digital Frequency Discriminators (DFD's).

The DR068 takes key performance elements from a number of existing production DFD's, integrating them for the first time into a complete digital solution suitable for military environments.

The DR068 offers the benefits of TDL's field-proven proprietary SSS discriminator tiers coupled with the latest digital technology to produce a receiver that not only measures frequency but is capable of Digital Signal Processing (DSP) of the raw frequency data.

DSP capability, is incorporated as standard; however, due to the use of state-of-the-art FPGA technology, TDL is able to adapt and add to the DSP capability to offer a DFD that is suitable for the majority of systems. In addition to measuring frequency, the DR068 also measures pulse parameters such as time of arrival (TOA), pulse width (PW) and pulse amplitude.

POP and FMOP options available on request.

Data is output as a 96 bit Pulse Descriptor Word (PDW) as three 32 bit words via the industry standard Front Panel Data Port (FPDP) connector. An optional 51 Way MDM interface is available.

The DFD is packaged in an industry standard dual slot (8HP) width plug-in format with DIN41612 interface for VME bus applications, suitable for most modern day EW suite equipment racks.

### FEATURES

- Broadband operation : 2-18 GHz
- 15-BIT output (0.5 MHz Resolution)
- Pulse Amplitude, Pulse Width and TOA
- 50 MHz Clocking rate
- 60 dB Dynamic range
- 'VME64' Form Factor

### APPLICATIONS

- Electronic Support Measures (ESM)
- Radar Warning Receivers (RWR)
- ECM Set-on
- Airborne, Fixed Wing & Rotary
- Land
- Naval



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## ELECTRICAL SPECIFICATIONS

| Ref | Parameter | Units | Value | | |
|---|---|---|---|---|---|
| | | | Min | Nom | Max |
| 1 | Operating Frequency Range | GHz | 2.00 | | 18.00 |
| 2 | Operating + Guard Band | GHz | 1.98 | | 18.02 |
| 3 | Unambiguous Frequency Range | GHz | 1.98 | 3.93 | 18.02 |
| 4 | Frequency Resolution | MHz | | 12 | |
| 5 | Digital Frequency Resolution | Bits | | | |
| 6 | Frequency Error (RMS) | MHz | | | 3.0 |
| 7 | Frequency Peak Error | MHz | | | 16 |
| 8 | Peak Error Rate | % | | | 0.04 |
| 9 | Frequency and Amplitude Measurement Dynamic Range | dBm | -55 | | 10 |
| 10 | Typical POI at –50dBm | | | | |
| 11 | External noise input | dBm | | | |
| 12 | Amplitude Resolution | dBm | | | |
| 13 | Digital Amplitude Resolution | Bits | | 100 | |
| 14 | Amplitude accuracy | dB rms | | | 2 |
| 15 | Recovery Time | ns | | | 500 |
| 16 | RF Input Pulse Width | ns | 50 | | CW |
| 17 | RF Input VSWR | | | | 2.1:1 |
| 18 | Clock Frequency (internal) | MHz | 49.5 | | 50.5 |
| 19 | Overload Power | dBm | | | 20 |
| 20 | Data Output Format | | Pulse descriptor word– frequency, amplitude, TOA, pulse width, bad data flags | | |
| 21 | Interfaces | Power-<br>Data Transfer-<br>RF input-<br>Audio output- | VME backplane<br>Front Panel dataport<br>SMA<br>Audio jack | | |
| 22 | Temperature Range | °C | -40 | | 85 |
| 23 | Power Supply Current | mA | | 900 | |
| 24 | Power Supply Current | A | | 3.0 | |
| 25 | Power Supply Current | A | | 1.0 | |
| 26 | Power Supply Current | mA | | 400 | |
| 27 | Weight (Approx.) | kg | | | 1.5 |
| 28 | Size (Approx.)<br>Length<br>Width (8HP)<br>Height (6U) | <br>mm<br>mm<br>mm | | <br>175<br>41.14<br>262 | |
| 29 | Boot Up Time | sec | | 5 | |



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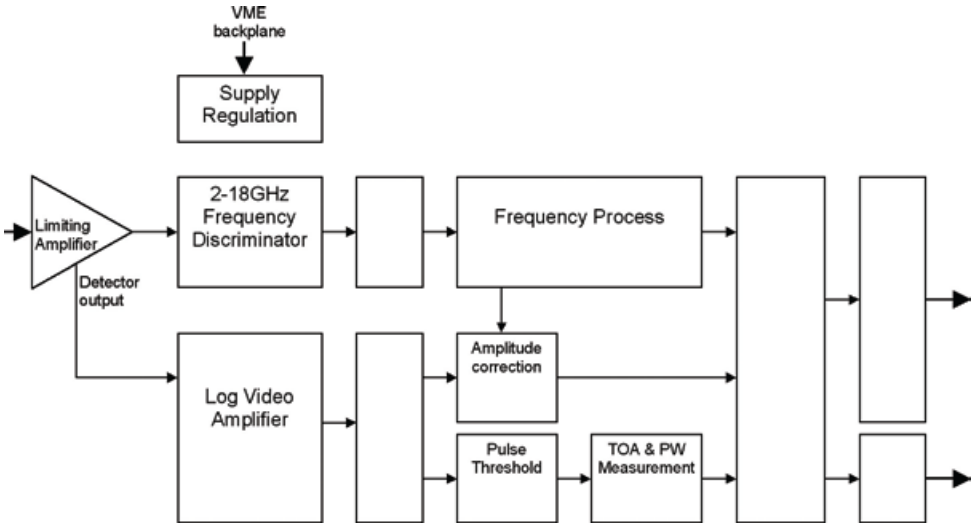
## BLOCK DIAGRAM

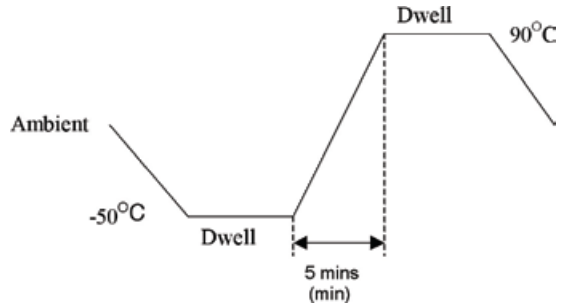



## ENVIRONMENTAL PERFORMANCE

The unit is designed to meet the environmental conditions specified below.

## TEMPERATURE

Absolute operating limits: –40ºC to +85ºC (standard VME rack with forced air cooling)
Storage temperature: –5OºC to +100ºC
Thermal cycling, survival: 5 cycles to the profile shown below –



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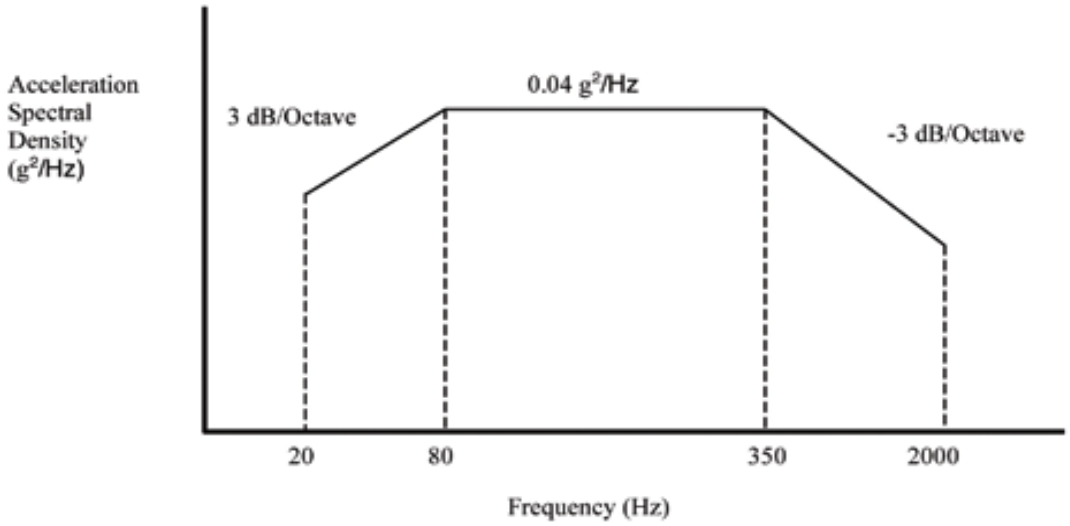
## HUMIDITY
Operational: Humidity level not exceeding 95% RH (non-condensing during operation).

## PRESSURE
Operational range: of 0.6 to 1.4 bar.
Storage range: 0.3 to 1.4 bar.

## VIBRATION
The unit is designed to meet the following vibration profile carried out on the worst axis: i.e. the force is perpendicular to the components.




## ACCELERATION
Structural survival: 6.75g in all directions.
Operational: 4.5g in all directions

## SHOCK
Survival: Terminal peak saw-tooth pulse with a peak value of 20g and duration 11 ms.

## RELIABILITY
The unit has a target MTBF of 25,000 hours for an Airborne Inhabited environment.

## ELECTROMAGNETIC COMPATIBILITY
The unit is designed with regard to the requirements of MIL STD 461E. Compliance can only be satisfied by careful design of the overall system particularly with regard to the interconnects between the DIFM and other parts of the system. While the design will be executed with regard to the requirements of the relevant standards, TDL cannot guarantee compliance if used inappropriately.



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## CONNECTOR INFORMATION

RF Input is via Front Panel sma(f) connector
Data Output via FPDP as detailed in Electrical Interface and Timing Information
DC Power via VME Backplane

## ELECTRICAL INTERFACE AND TIMING

The primary interface for pulse measurement information is the Front Panel Data Port. This port is designed in accordance with VITA 17-199x Rev 1.7 (24 Nov 1998).

The general operation is as described below:

- The DR068 transmits a Pulse Descriptor Word on the FPDP every time an RF pulse is detected and measured.
- The FPDP communication is one-way, however, the receiver is able to suspend transmission of PDW's by asserting
- the SUSPEND signal.
- The FPDP data word is 32-bit wide 'frame', a DR068 PDW is 96-bits long, therefore 3 32-bit frames are
- transmitted for every PDW
- The FDPD clock rate is 40MHz.
- A PDW transfer takes 5 clock cycles, therefore at 40MHz, it takes 125ns to TX a PDW.

NOTE: The DR068 has been designed and tested using a PC driven FPDP card, this card is manufactured by VMETRO
(model number DPI02-FBU)

The following table defines a format for a pulse descriptor word:

| Parameter | No of Bits | Resolution | Description |
|---|---|---|---|
| **Parameter** | No of Bits | Resolution | Maximum Value |
| **Frequency** | 15 | | |
| **Amplitude** | 8 | | |
| **Pulse Width** | 16 | 5ns | 327.675us |
| **Time of Arrival** | 32 | 5ns | 21.47s |
| **Flags** | 6 | | |

The format of the data frame will be as follows:

| | | | |
|---|---|---|---|
| **Word 0** | TOA [D31:0] | | |
| **Word 1** | Pulsewidth [D31:16] | Frequency [D15:1] | Spare [D0] |
| **Word 2** | Flags [D31:26] | Spare [D25:8] | Amplitude [D7:0] |



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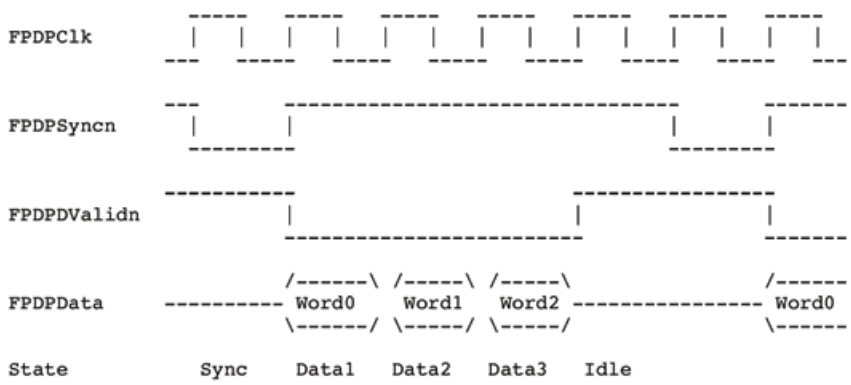
Flag data is as follows:

| | | | |
|---|---|---|---|
| D31 | Bad Data – ambiguity | D30 | Bad data – threshold |
| D29 | Not used | D28 | Not used |
| D27 | CW Flag | D26 | Not used |

Front Panel Data transfer:
Each PDW will be transferred in five front panel data port clock cycles. The DR068 is the master (transmitter) the host system is the slave (receiver).

The diagram below shows a full transfer plus start of next transfer.




NOTE: Refer to Front Panel Data Port Specifications, VITA 17-199x, for details of operation of the transfer bus.

## NOTES

1. The pulse width measurement will be derived from the output signal of the pulse detection circuit, i.e. it will not be the width of pulse at 3 dB points.
2. Pulse widths longer than the maximum specified will be flagged as CW. A PDW will be generated at the end of every 327.675us (with the CW flag set) until the pulse has been determined to have gone away.
3. The TOA counter will roll-over to zero every 21.47s.



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